Guest Editorial Special Section on the International Symposium on Circuits and Systems—ISCAS 2025

THIS Special Section of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI) features selected articles invited from the *IEEE International Symposium on Circuits and Systems* (ISCAS) 2025[1], held on May 25–28, 2025, in London, U.K. ISCAS is the flagship conference of the IEEE Circuits and Systems Society (CASS). The theme of ISCAS 2025, "Technology Disruption and Society," emphasizes the role of technology and integrated electronic systems in developing innovative solutions to today's societal challenges. The symposium gathers experts across the broad circuits and systems community, showcasing high-quality research in analog and digital integrated circuits, power and energy systems, electronic design automation (EDA), biomedical circuits, sensor interfaces, communication systems, and more.

This year marks the first collaboration between TVLSI and ISCAS for a Special Section, in parallel with three other CASS journals: IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS (TCAS-I), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART II: EXPRESS BRIEFS (TCAS-II), and IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS (TBioCAS). Invitations to submit to TVLSI were extended by a team of guest associate editors based on the timeliness and quality of the technical contributions, the outcomes of the ISCAS review process, and the recommendations of review committee members (RCMs) and track chairs (TCs). The subsequent evaluation followed the standard TVLSI review procedure. The Guest Editor team overseeing this process consists of Prof. Aatmesh Shrivastava (Northeastern University, Boston, MA, USA), Prof. Lan-Da Van (National Yang Ming Chiao Tung University, Hsinchu, Taiwan), and Prof. Xinfei Guo (Shanghai Jiao Tong University, Shanghai, China).

This Special Section includes 12 accepted articles. Each manuscript underwent at least one round of revision, with a minimum of three reviewers per round. The review standards were maintained at the same rigor as those for regular TVLSI submissions, ensuring a thorough and high-quality evaluation process. Together, these 12 articles in this Special Section showcase the remarkable breadth of innovation presented at ISCAS 2025, spanning integrated circuits, systems, design automation, and emerging computing paradigms. The contributions range from high-voltage analog and mixed-signal circuit techniques, secure architectures, and cryogenic CMOS receivers, to advanced digital and memory-centric computing systems, including near-memory STT-MRAM macros, smart-vision system-on-chips (SoCs), and high-performance multi-in multi-out (MIMO) transceivers. Several articles highlight the growing impact of machine learning and reconfigurable computing on the circuits and systems community, with new field-programmable gate array (FPGA) accelerators, online-learning-based resource management, coordinated scheduling for mixture-of-expert models, and transformer-optimized processors. Others advance the EDA frontier through new datasets and benchmarks for PCB routing and novel approaches to quantum compilation. Collectively, these works reflect the multidisciplinary nature of modern VLSI and demonstrate how innovations across circuits, architectures, EDA, and intelligent systems continue to drive the field forward.

These articles also reflect emerging trends in the rapidly evolving VLSI field. TVLSI occupies a unique position within IEEE, being jointly sponsored by three societies, CASS, SSCS, and CS, which gives it the responsibility and opportunity to unify research topics, conference communities, and shared interests across these domains. Since 2024, TVLSI has broadened its outreach by collaborating with multiple flagship conferences from multiple societies, publishing selected articles as Special Issues or Special Sections. The present Special Section is one such example. These efforts align with the mission of the TVLSI editorial team, led by Prof. Mircea Stan, Editor-in-Chief, to attract the highest-quality research within the journal's scope. Over the past year, the editorial team has also worked diligently to streamline the review cycle and refine the journal's topical focus, thereby positioning TVLSI more strategically and reducing overlap with sister journals. In addition, "The Best of TVLSI" Webinar Series[2] has been launched since December 2024 to highlight excellent articles published in recent TVLSI issues. Notably, TVLSI recently received a "High Performance" rating from IEEE for the first time, recognizing the journal's improved operational efficiency. Combined with the fact that the Impact Factor has now surpassed 3 (reaching 3.1), these achievements underscore the strong collective efforts of the editorial board, steering committees, guest editors, reviewers, and contributing authors. We look forward to publishing more high-quality Special Issues or Sections that showcase the outstanding work of this vibrant community.

The preparation of this Special Section was made possible through close collaboration with the ISCAS 2025 Program Co-Chairs: Dr. Gabriele Manganaro, Dr. Maire O'Neill,

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[1]https://2025.ieee-iscas.org/

[2]https://ieee-cas.org/publication/tvlsi/best-tvlsi-webinar-series

Dr. Elena Blokhina, Dr. Timothy Constandinou, and Dr. Håkan Johansson, whose expertise, guidance, and insights were invaluable. We also extend our special gratitude to Dr. Gabriele Manganaro, Vice President of Publications of CASS, for his support of this collaboration. Finally, we sincerely thank Prof. Mircea Stan, Editor-in-Chief of IEEE TVLSI, and Stacey Weber, TVLSI administrative staff, for their exceptional dedication and professionalism, which were instrumental in the success of this Special Section.

Working with ISCAS 2025 has been a unique experience and a testament to completing complex tasks in a fast and highly efficient manner. We would like to express our sincere gratitude to all invited authors from around the world who contributed to this Special Section for their excellent articles and for their efforts in meeting the tight and demanding timeline required to bring this Special Section to publication on schedule. We are also deeply grateful to the more than 40 reviewers who participated in multiple review rounds; their constructive feedback and thoughtful recommendations significantly enhanced the readability and quality of the articles included here. With ISCAS 2026 approaching, we look forward to continuing this collaboration and to publishing more high-quality articles that benefit the research community and society at large.

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Xinfei Guo (Senior Member, IEEE) received the M.S. degree in electrical and computer engineering from the University of Florida, Gainesville, FL, USA, in 2012, and the Ph.D. degree in computer engineering from the University of Virginia, Charlottesville, VA, USA, in 2018.

Before joining academia, he worked at NVIDIA, Westborough, MA, USA, and IBM Research, Yorktown Heights, NY, USA, where he was a key member to contribute to multiple chip products, including the world-leading BlueField data processing units (DPUs) and a total of seven chip tapeouts that cover a wide range of technology nodes from 180 to 7 nm. He is currently an Associate Professor with the Global College, Shanghai Jiao Tong University (SJTU), Shanghai, China, where he leads the Intelligent Circuits, Architectures and Systems (iCAS) Laboratory. His previous work has resulted in over 50 conference papers or journal articles and holds six patents in circuit design, electronic design automation (EDA), or field-programmable gate array (FPGA) fields. He also published a book and a book chapter. His team currently focuses on low-power and high-reliability computing, machine learning-assisted EDA techniques, and edge-computing architectures.

Dr. Guo received the best paper awards as the co-author from the IEEE System on Chip Conference (SOCC) in 2022, the IEEE Latin America Symposium on Circuits and Systems (LASCAS) in 2019, and the IEEE Workshop on Silicon Errors in Logic—System Effects (SELSE) in 2017. He received multiple best presentation awards at various conferences. He was a recipient of the 2017 IEEE Circuits and Systems Society (CASS) Pre-Doctoral Fellowship. He serves as an Associate Editor-in-Chief (AEiC) for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, an Associate Editor for *Integration*, the VLSI Journal, and a program committee member or the chair for over ten IEEE/ACM conferences in design and EDA fields.

Lan-Da Van (Senior Member, IEEE) received the B.S. (Hons.) and M.S. degrees from the Tatung Institute of Technology, Taipei, Taiwan, in 1995 and 1997, respectively, and the Ph.D. degree from the National Taiwan University, Taipei, in 2001, all in electrical engineering.

From 2001 to 2006, he was an Associate Researcher with the National Chip Implementation Center, Hsinchu, Taiwan. Since 2006, he has been with the Department of Computer Science, National Yang Ming Chiao Tung University (NYCU), Hsinchu, where he served as the Associate Director of the Microelectronics and Information Research Center from 2021 to 2025, has been the Director of the EECS International Graduate Program since 2023, and is currently a Professor. He has published over 80 articles, co-authored the book *Online Component Analysis, Architectures and Applications* in 2022, and his publications have over 1600 citations on Google Scholar. His research interests include VLSI-DSP algorithms, architectures, and systems, covering low-power/high-performance adaptive filters, computer arithmetic, graphics systems, ICA, machine/deep learning, multidimensional filters, and transforms.

Dr. Van has received multiple recognitions, including the Best Poster Award at iCEER 2005 and the Best Paper Award at IEEE iThings 2014. He has held numerous IEEE leadership roles, including the Chair of the IEEE CASS VLSI Systems and Applications Technical Committee from 2024 to 2026 and representative to the IEEE Council on RFID from 2024 to 2025. He has served as the Program/Session Chair for major conferences such as ISCAS, AICAS, SOCC, ISOCC, MCSoC, and APCCAS, and an Associate Editor for IEEE TRANSACTIONS ON COMPUTERS, IEEE ACCESS, IEEE INTERNET OF THINGS JOURNAL, *ACM Computing Surveys*, and IEEE TRANSACTIONS ON EMERGING TOPICS IN COMPUTING. He is also a Higher Education Academy (HEA) Fellow.

Aatmesh Shrivastava (Senior Member, IEEE) received the Ph.D. degree from the University of Virginia, Charlottesville, VA, USA, in 2014.

From 2006 to 2010, he was a Senior Design Engineer with Texas Instruments, Bengaluru, India. From 2014 to 2016, he worked as the Senior Design Director with Everactive, Charlottesville, VA, USA, the Internet of Things (IoT) start-up, where he led the research and development of the energy harvesting and power management solutions. In August 2016, he joined Northeastern University, Boston, MA, USA, where he is currently an Associate Professor with the Department of Electrical and Computer Engineering. His research interests include self-powered and ultralow-power circuits and systems, energy harvesting and analog computing, hardware for AI, the IoT, and ultralow-power biomedical and neural circuits.

Dr. Shrivastava was a recipient of the DARPA Young Faculty Award in 2023, the NSF CAREER Award in 2022, the Acorn Innovation Award from Mass Ventures in 2021, and the 2024 Faculty Fellow Award from the College of Engineering, Northeastern University. He was also a recipient of the 2024 Distinguished Alumni Award from his alma mater, BIT Mesra, India. He served as an Associate Editor on the editorial board for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, from 2023 to 2024. He currently serves as an Associate Editor for IEEE OPEN JOURNAL ON CIRCUITS AND SYSTEMS and a Senior Editor for IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS.